The Rejections

35 USC § 112, first paragraph

Claims 1-4, and 8-19 were rejected under 35 U.S.C. 112, first paragraph, on the basis that:

> [These claims contain] subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "an internal capacitor" can be found. While the applicant has pointed out that support for "an internal capacitor" "appears in the specification at, e.g., p.l., lines 1-2 (integrated capacitor) and Fig. 3, 5, and 6," it is not clear that a recitation of an "integrated capacitor". Nor is it clear how figures 3, 5, and 6, which depict an integrated capacitor, depict support for "an internal capacitor."

Applicants have amended claim 1 to replace the term "internal" with "embedded," which is a term understood in the art to mean a capacitor positioned between other layers in an electronic package, such as the capacitor disclosed in Figs. 3, 5, and 6 of the present application.

Based on the foregoing, Applicants submit the rejections of claim 13 under 35 U.S.C. § 112, first paragraph, should be withdrawn.

35 USC § 112, second paragraph

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

> It is not clear if the limitation "the non-conductive polymer is blended with high dielectric constant particles" is referring to the same "high dielectric constant particles as claimed in claim 1. For purposes of this office action "the non-conductive polymer is blended with high dielectric constant particles" will be considered --the high dielectric constant particles are --

Applicants have amended claim 13 to clarify its meaning.

Based on the foregoing, Applicants submit the rejections of claim 13 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

35 USC § 103 - Kabumoto (U.S. Pat. No. 5,883,428) in view of Brandt (U.S. Pat. No. 6,068,782) and Parker (U.S. Pat. No. 5,633,785).

Claims 1 -3, 8 -13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto in view of Brandt and Parker.

The Office Action states in part:

> Kabumoto discloses in figure 1 an electronic package (4). Kabumoto discloses in figure 1 a conductive trace layer (5) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads (5a and 5b). Kabumoto discloses in figure a dielectric substrate (portion of 1 above 5) mounted on the first side of the conductive trace' layer. Kabumoto discloses in figure an internal capacitor including a first conductive layer (10), a second conductive layer (11) and a layer of dielectric material (portion of 1 between 10 and 11) disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer (portion of 1 between 10 and 5).
>
> Kabumoto discloses in figure 1 a plurality of interconnect regions (12a -12d) extending through the first conductive layer and the dielectric material layer of the capacitor. Kabumoto discloses in figure an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected (12a) to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected (12b) to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

According to MPEP 2142, to establish a case of prima facie obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) the prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co., 226 USPQ 438 (PTO Bd. App. 1984).*

Applicants respectfully submit that the cited references cannot support a case of *prima facie* obviousness as to the claims because, among other possible reasons, the cited references do not provide a motivation or suggestion for using an embedded capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. and having a dielectric layer made of a non-

conductive polymer blended with high dielectric constant particles. Applicants base their position on the following:

As stated in *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 USPQ 657 (Fed. Cir. 1985):

> To combine references (A) and (B) properly to reach the conclusion that the subject matter of a patent would have been obvious, case law requires that there must be some teaching, suggestion, or inference in either reference (A) or (B), or both, or knowledge generally available to one of skill in the art to combine the relevant teachings of references (A) and (B). Consideration must be given to teachings in the references that would have led one skilled in the art away from the claimed invention. A claim cannot properly be used as a blue print for extracting individual teachings from a reference (emphasis added).

Kabumoto teaches away from using internal (i.e., embedded) capacitors at col. 2, lines 43-54:

> [S]ince the specific dielectric constant of the sintered aluminum oxide which composes the insulating substrates of semiconductor element-housing packages is as low as approximately 7, it becomes necessary to have a great number of pairs of ground planes [**10**] and power-supply planes [**11**] placed opposing each other and sandwiching part of the insulating layers which form the insulating substrate [**1**], or to have vast opposing areas of the paired ground planes and power-supply planes, in order to store sufficiently increased capacitance between the paired ground planes and power-supply planes as decoupling capacitors, and this creates the drawback that extremely thick, large and heavy packages are required for housing a semiconductor element.

Kabumoto instead teaches the use of an external capacitor (chip capacitor **9**) with ground plane **10** and power-supply plane **11** functioning as conducting paths:

> "The ground plane **10** and the power-supply plane **11** [] function as conducting paths to electrically connect the respective electrodes of the chip capacitor **9** to the ground bonding pad **5*a*** and the power-supply bonding pad **5*b*** [.] (Col. 6, lines 17-21) . . . [In combination with the other

> elements of the system this allows] normal operation of the semiconductor element **3** without preventing reduction in power-supply noise by the chip capacitor **9**. (Col. 6, lines 36-39)

In response to Applicant's previously submitted arguments, the present Office Action states in part:

> With regard to the applicant's argument that "Kabumoto teaches away from using internal capacitors to achieve higher capacitance," it should be noted that the capacitor in figure 1 of Kabumoto is an internal capacitor.

Applicants submit that this statement mischaracterizes the teachings of Kabumoto. While the power and ground plane may inherently have capacitance between them, Kabumoto does not teach using this structure as a capacitor. Applicants submit that the Examiner is inappropriately trying to support a finding of obviousness by using an argument that addresses novelty. As stated in *Jones v. Hardy*, 220 USPQ 1021, 1025 (Fed. Cir. 1984), though anticipation is the epitome of obviousness, they are separate and distinct concepts.

Another portion of the office action states:

> Kabumoto does not disclose that the dielectric material is made of a nonconductive polymer blended with high dielectric particles. Brandt discloses in column 4, lines 18 -41 a dielectric material made of a non-conductive polymer blended with high dielectric particles. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material of Brandt in the method of Kabumoto in order to tune the electronic properties of a capacitor component as stated by Brandt in column 4, lines 22 -41.

Applicants submit that it would not have been obvious to use the dielectric materials of Brandt in the method of Kabumoto "to tune the electronic properties of a capacitor component" when the capacitor is an embedded capacitor because (1) Kabumoto does not teach (and, in fact, teaches away from) an embedded capacitor component and (2) Brandt only mentions "tuning" electronic properties in connection with using more than one layer of different materials. (Col. 4, lines 37-41.) It does not state that the mere use of certain materials will "tune" the electronic properties of a capacitor.

Furthermore, it would not have been obvious to substitute the polymeric dielectric material of Brandt for the inorganic dielectric material of Kabumoto because using the polymeric materials of Brandt in the process of Kabumoto would require a completely new process. Brandt

uses a sequential build-up method to form its capacitor structure, whereby each layer is deposited on the previous layer. (*See, generally*, Brandt, Abstract, lines 3-4; *see also* Brandt col. 3, lines 25-28 and 31-34; and col. 4, lines 28-35.) In contrast, Kabumoto uses a method wherein the insulating layers are formed first into ceramic sheets (*see* Kabumoto, col. 4, lines 7-18), then the conductive layers are applied as a patterned powder or paste to the ceramic sheets and sandwiched between other ceramic sheets, then the sandwiched layers are fired together to form the insulating substrate (*see* Kabumoto, col. 6, lines 48-67).

Another portion of the office action states:

> Kabumoto and Brandt are silent to the capacitor having a capacitance of from about to about 100 nf/sq.cm. Parker teaches in figure 4, column 5, lines 43 -50 and column 7, lines 4 -12 a capacitor with a capacitance of about 10 nf/sq.cm. It would have been obvious to one of ordinary skill in the art at the time of the present invention to have the capacitance of Parker in the package of Kabumoto and Brandt in order to provide a capacitance which is sufficient for capacitive decoupling in a package as stated by Parker in column 7, lines 8 -12.

And in response to Applicant's previously submitted arguments the Office Action states in part:

> With regard to the applicant's arguments that "there is no motivation to use the high capacitance internal capacitor of Parker in the Kabumoto structure," it should be noted that the internal capacitor of Parker is not being substituted into the Kabumoto structure. In fact, Parker is being used in combination with Kabumoto and Brandt to show that an internal capacitor can have a capacitance of the claimed range. For example, Kabumoto and Brandt are silent to the capacitance of their capacitor. Therefore the applicant's argument is not persuasive, and the rejection is proper.

Applicants submit that it would not be obvious to "have the capacitance of Parker in the package of Kabumoto and Brandt" because, as previously stated, Kabumoto teaches away from using an embedded capacitor. The Examiner cites Parker for teaching sufficient capacitance for capacitive coupling in an embedded capacitor, but completely ignores the fact that Kabumoto teaches away from using embedded capacitors and teaches the use of an external capacitor.

Furthermore, Parker (and Kabumoto) only teaches the use of high dielectric materials (e.g., sintered aluminum oxide) as its insulating layer. It does not teach the use of a polymer/ceramic composite. Accordingly, the capacitance of the Parker structure provides no indication of the capacitance that would be obtained by using the Brandt polymer/ceramic composite material. As the Examiner states, Brandt is silent to the capacitor having a

capacitance of from about 1 to about 100 nf/sq.cm. Therefore, it would not be known at the time the invention was made that a combination of the teachings from Kabumoto and Brandt would produce a capacitor "having" a capacitance of from about 1 to about 100 nf/sq.cm.

The Examiner cites *In re McLaughlin*, 170 USPQ 209 (CCPA 1971) for the proposition that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. However, Applicants note that *In re McLaughlin* also states that the tests for combining references is not what the individual references themselves suggest, but rather what the combination of disclosures, taken as a whole, would suggest to one of ordinary skill in the art.

Applicants submit that when the references are considered in combination, and taken as a whole, they do not suggest the presently claimed invention to one of ordinary skill in the art.

For these reasons, Applicants submit that the cited references will not support a 103(a) rejection of the claims invention and request that the rejection be withdrawn.

35 USC § 103 - Kabumoto (U.S. Pat. No. 5,883,428) in view of Brandt (U.S. Pat. No. 6,068,782) and Parker (U.S. Pat. No. 5,633,785) and further in view of Dehaine (U.S. Pat. No. 4,982,311).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto, Brandt, and Parker as applied to claims 1 and 3 above, and further in view of Dehaine.

The Office action states in part:

> Kabumoto discloses in figure 1 a device receiving region extending through the dielectric substrate and the conductive trace layer and further comprises an electronic device (3) attached to the device receiving region on 1he stiffening member by a third adhesive layer (la). Kabumoto, Brandt and Parker are silent to the device-receiving region also extends through the capacitor and further comprises the electronic device mounted on the stiffening member. Dehaine discloses in figure a device receiving region extending through a dielectric substrate (16), a conductive trace layer (34b), a capacitor (18a and 18b), and further comprises an electronic device (12) attached to the device

> receiving region on a stiffening member (20) by a third adhesive layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the receiving region of Dehaine in the device of Kabumoto, Brandt, and Parker in order to allow easy refrigeration of the electronic device as stated by Dehaine in column 2, lines 33-40. It is known that electronic devices such as semiconductor elements run more efficiently at reduced temperatures.

Applicants respectfully point out several errors made by the Examiner in describing what is disclosed by the references:

In Kabumoto, element 1a is not an adhesive layer, it is as a mounting portion of substrate 1.

In Dehaine, 18a and 18b are not parts of a capacitor. Element 19 is the capacitor. 18a and 18b are conductor faces connected to capacitor 19.

In any event, the addition of Dehaine to the combination of Kabumoto, Brandt, and Parker does not overcome the failure of the combination of these three references, as described above, to support a 103 rejection of the claimed invention.

For these reasons, Applicants submit that the cited references will not support a 103(a) rejection of the claims invention and request that the rejection be withdrawn.

35 USC § 103 - Kabumoto (U.S. Pat. No. 5,883,428) in view of Brandt (U.S. Pat. No. 6,068,782) and Parker (U.S. Pat. No. 5,633,785) and further in view of Fujisawa et al. (U.S. Pat. No. 6,184,567).

Claims 14-16, 18 and 19 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Kabumoto, Brandt, and Parker as applied to claims 1 and 3 above, and further in view of Fujisawa.

The office action states in part:

> With regard to claim 14 . . . It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plurality of apertures of Fujisawa in the device of Kabumoto, Brandt, and Parker in order to ensure insulation between contact pads of the trace layer.

> With regard to claims 15 and 16 . . . it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the polyamide film of Fujisawa in the device of Kabumoto,

> Brandt, and Parker in order to resist moralization while bonding to the electronic device.
>
> With regard to claim 18 . . . it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solder pad of Fujisawa as the interconnect pad in the device of Kabumoto, Brandt, and Parker in order to use flip chip bonding for the connection.
>
> With regard to claim 19 . . . it would have been further obvious in the method of Kabumoto, Parker and Fujisawa that the dielectric substrate has an aperture extending there through adjacent each solder ball pad.

Applicants submit that the addition of Fujisawa to the combination of Kabumoto, Brandt, and Parker does not overcome the failure of the combination of these three references, as described above, to support a 103 rejection of the claimed invention.

For these reasons, Applicants submit that the cited references will not support a 103(a) rejection of the claims invention and request that the rejection be withdrawn.

In addition to the foregoing arguments, Applicants submit that a dependent claim should be considered allowable when its parent claim is allowed. *In re McCain*, 1012 USPQ 411 (CCPA 1954). Accordingly, provided the independent claims are allowed, all claims depending therefrom should also be allowed.

Based on the foregoing, it is submitted that the application is in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 112 and 103 is requested. Examination and reconsideration of the claims are requested. Allowance of the claims at an early date is solicited.

If there are any matters that may be resolved or clarified through a telephone interview, the Applicants' Attorney makes herself available at the telephone number listed below. Alternately, the Examiner may fax communications directly to the Applicants' Attorney at the facsimile number listed below.

The Applicants believe that no fees are necessary in relation with the filing of the present communication. If the Applicants are mistaken, the Applicants hereby authorize the Commissioner to deduct any additionally required fees from or credit any overpayment to Deposit Account 13-3723.

The Examiner is invited to contact Applicants' attorney if the Examiner believes any remaining questions or issues could be resolved.

Respectfully submitted,

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Date

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Version of claims showing changes made

1.(Four times Amended). An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a dielectric substrate mounted on the first side of the conductive trace layer;

an [internal] embedded capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. including a first conductive layer, a second conductive layer and a layer of dielectric material made of a non-conductive polymer blended with high dielectric constant particles disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

13. (Twice Amended) The electronic package of claim 1 wherein the [non-conductive polymer is blended with] high dielectric constant particles are formed from a material selected from the group consisting of barium titanate, barium strontium titanate, titanium oxide, lead zirconium titanate and tantalum oxide.